



MODEL NO. : TS104SAALC01-00

ISSUED DATE: 2008-05-07

VERSION : Ver 1.0

- Preliminary Specification
- Final Product Specification

Customer : \_\_\_\_\_

Approved by	Notes

This technical specification is subjected to change without notice

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## 1 General specifications

Feature		Spec
<b>Display Spec.</b>	Size	10.4 inch
	Resolution	800(RGB) X 600
	Interface	LVDS 6 bit
	Color Depth	262k
	Technology type	a-si TFT
	Pixel pitch (mm)	0.264*0.264
	Pixel Configuration	R.G.B. Vertical Stripe
	Display Mode	TM with Normally White
	Surface Treatment(Up Polarizer)	Anti-Glare
	Viewing Direction	12 o'clock
	Gray Scale Inversion Direction	6 o'clock
<b>Mechanical Characteristics</b>	DIM. LCM (W x H x D) (mm)	236*176.9*5.6
	Active Area(mm)	211.2*158.4
	With /Without TSP	Without TSP
	Weight (gram)	TBD.

Note 1 : Viewing direction for best image quality is different from TFT definition, there is a 180 degree shift.

Note 2 : Requirements on Environmental Protection: RoHS



## 2 Input/Output terminals

### 2.1 LVDS interface

Connector type: HIROSE DF19K-20P-1H (56)

No	Symbol	I/O	Description	Comment
1	VDD	P	Power Supply	
2	VDD	P	Power Supply	
3	GND	P	Ground	
4	GND	P	Ground	
5	IN0-	I	LVDS receiver negative signal channel 0	Note1
6	IN0+	I	LVDS receiver positive signal channel 0	Note1
7	GND	P	Ground	
8	IN1-	I	LVDS receiver negative signal channel 1	Note1
9	IN1+	I	LVDS receiver positive signal channel 1	Note1
10	GND	P	Ground	
11	IN2-	I	LVDS receiver negative signal channel 2	Note1
12	IN2+	I	LVDS receiver positive signal channel 2	Note1
13	GND	P	Ground	
14	CLK-	I	LVDS receiver negative signal clock	
15	CLK+	I	LVDS receiver positive signal clock	
16	GND	P	Ground	
17	NC	-	No connection	
18	NC	-	No connection	
19	GND	P	Ground	
20	GND	P	Ground	

P: Power/GND; I: input pin;

Table 2.1 input terminal pin assignment

Note1: Data mapping as follows:

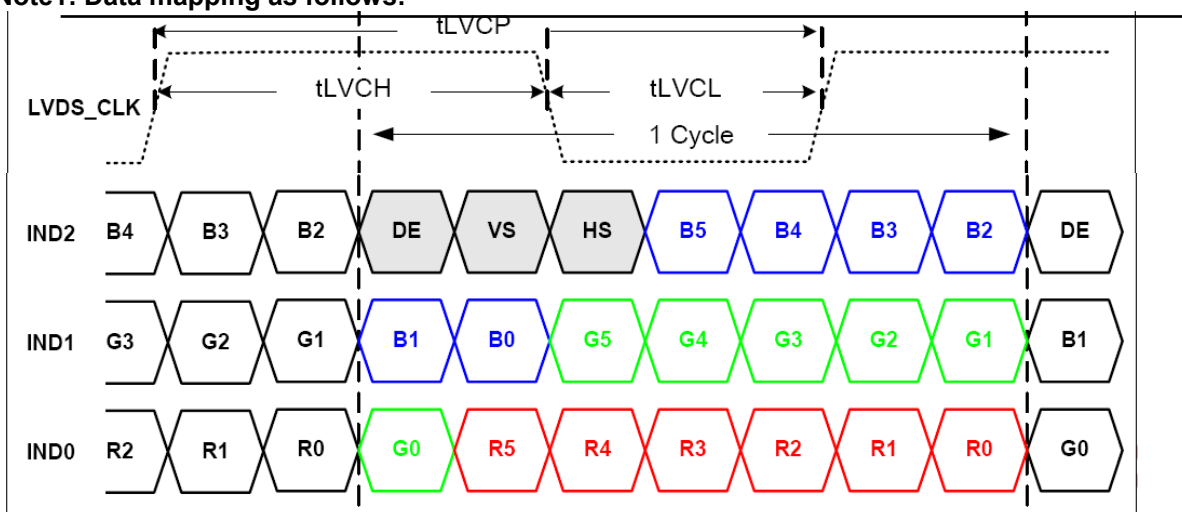


Figure 2.1 Input signal data mapping

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## 2.2 CN1 and CN3 pin assignment of FPC

No	Symbol	I/O	No	Symbol	I/O	No	Symbol	I/O
1	DUMMY	-	34	EDGSL	I	67	V13	I
2	DUMMY	-	35	SHL	I	68	V14	I
3	XON_G	I	36	CLK	I	69	AVSS	P
4	GND_G	P	37	CLKN	I	70	AVSS	P
5	GND_G	P	38	D00	I	71	AVSS	P
6	VCC_G	P	39	D01	I	72	AVSS	P
7	VCC_G	P	40	D02	I	73	D20	I
8	VEE_G	P	41	D03	I	74	D21	I
9	VEE_G	P	42	D04	I	75	D22	I
10	DUMMY	-	43	D05	I	76	D23	I
11	VGG_G	P	44	D10	I	77	D24	I
12	VGG_G	P	45	D11	I	78	D25	I
13	STVU_G	I	46	D12	I	79	LD	I
14	STVD_G	I	47	D13	I	80	REV	I
15	CKV_G	I	48	D14	I	81	POL	I
16	U/D_G	I	49	D15	I	82	VCC	P
17	OE_G	I	50	DUMMY	-	83	VCC	P
18	VCOM	I	51	AVDD	P	84	VCC	P
19	VCOM	I	52	AVDD	P	85	GND	P
20	VCOM	I	53	AVDD	P	86	GND	P
21	VCOM	I	54	AVDD	P	87	GND	P
22	DIO1	I/O	55	V1	I	88	ENREOP	I
23	AVSS	P	56	V2	I	89	AVDD	P
24	AVSS	P	57	V3	I	90	AVDD	P
25	AVSS	P	58	V4	I	91	AVDD	P
26	AVSS	P	59	V5	I	92	AVDD	P
27	GND	P	60	V6	I	93	DUMMY	-
28	GND	P	61	V7	I	94	DIO2	I/O
29	GND	P	62	V8	I	95	VCOM	I
30	VCC	P	63	V9	I	96	VCOM	I
31	VCC	P	64	V10	I	97	VCOM	I
32	VCC	P	65	V11	I	98	VCOM	I
33	TTLRSDS	I	66	V12	I			

P: Power/GND; I: input pin; I/O: input or output pin;

**Table 2.2 CN1 and CN3 pin assignment**

**2.3 CN2 and CN4 pin assignment of FPC**

No	Symbol	I/O	No	Symbol	I/O	No	Symbol	I/O
1	DUMMY	-	34	D02	I	67	D20	I
2	DUMMY	-	35	D03	I	68	D21	I
3	DUMMY	-	36	D04	I	69	D22	I
4	DUMMY	-	37	D05	I	70	D23	I
5	DUMMY	-	38	D10	I	71	D24	I
6	DUMMY	-	39	D11	I	72	D25	I
7	DUMMY	-	40	D12	I	73	LD	I
8	DUMMY	-	41	D13	I	74	REV	I
9	VCOM	I	42	D14	I	75	POL	I
10	VCOM	I	43	D15	I	76	VCC	P
11	VCOM	I	44	DUMMY	-	77	VCC	P
12	VCOM	I	45	AVDD	P	78	VCC	P
13	DUMMY	-	46	AVDD	P	79	GND	P
14	DUMMY	-	47	AVDD	P	80	GND	P
15	DUMMY	-	48	AVDD	P	81	GND	P
16	DIO1	I/O	49	V1	I	82	ENREOP	I
17	AVSS	P	50	V2	I	83	AVDD	P
18	AVSS	P	51	V3	I	84	AVDD	P
19	AVSS	P	52	V4	I	85	AVDD	P
20	AVSS	P	53	V5	I	86	AVDD	P
21	GND	P	54	V6	I	87	DUMMY	-
22	GND	P	55	V7	I	88	DIO2	I/O
23	GND	P	56	V8	I	89	DUMMY	-
24	VCC	P	57	V9	I	90	DUMMY	-
25	VCC	P	58	V10	I	91	DUMMY	-
26	VCC	P	59	V11	I	92	DUMMY	-
27	TTLRSDS	I	60	V12	I	93	VCOM	I
28	EDGSL	I	61	V13	I	94	VCOM	I
29	SHL	I	62	V14	I	95	VCOM	I
30	CLK	I	63	AVSS	P	96	VCOM	I
31	CLKN	I	64	AVSS	P	97	DUMMY	-
32	D00	I	65	AVSS	P	98	DUMMY	-
33	D01	I	66	AVSS	P			

P: Power/GND; I: input pin; I/O: input or output pin;

**Table 2.3 CN2 and CN4 pin assignment**

**4.4 CN5 (CCFL connector)**

No	Symbol	I/O	Description	Comment
1	VL1	P	CCFL power supply(high voltage)	
2	VL2	P	CCFL power supply(GND)	

**3 Absolute maximum ratings**

GND=0V, Ta = 25°C

Item	Symbol	MIN	MAX	Unit	Remark
Power Voltage	VDD	-0.3	5	V	
	AVDD	-0.5	15	V	
	VGH	-0.3	42	V	
	VEE	-20	0.3	V	
	VGH-VEE	-0.3	40	V	
Input voltage	V <sub>IN</sub>	-0.3	5	V	
Operating Temperature	Top	-20	70	°C	
Storage Temperature	Tst	-30	80	°C	

**Table 3.1 absolute maximum rating**



## 4 Electrical characteristics

### 4.1 LVDS DC Electrical Characteristics

GND=0V, Ta=25°C

Item	Symbol	MIN	TYP	MAX	Unit	Remark
LVDS Differential input high threshold	$V_{TH}$	-	-	+100	mV	$V_{CMLVDS}=1.2V$
LVDS Differential input low threshold	$V_{TL}$	-100	-	-	mV	$V_{CMLVDS}=1.2V$
Differential input voltage	$ V_{ID} $	0.1	-	0.6	V	
LVDS input common mode voltage	$V_{CMLVDS}$	$ V_{ID} /2$	1.25	$1.4-( V_{ID} /2)$	V	
Input current	$I_{IN}$	-10	-	10	uA	

Table 4.1 LVDS DC Electrical Characteristics

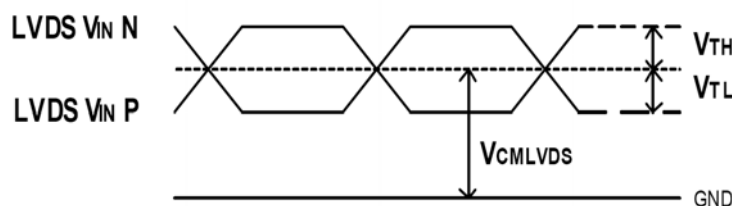


Figure 4.1 LVDS DC timing diagram

### 4.2 LCD module

GND=0V, Ta=25°C

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Supply Voltage	VDD	3.0	3.3	3.6	V	
Analog supply Voltage	AVDD	TBD.	9.8	TBD.	V	
Gate on voltage	VGH	TBD.	22.0	TBD.	V	
Gate off voltage	VEE	TBD.	-7.0	TBD.	V	
Input Signal Voltage	Low Level	$V_{IL}$	0	-	0.8	V
	High Level	$V_{IH}$	$0.7 \cdot VDD$	-	VDD	V
Output Signal Voltage	Low Level	VOL	-	-	0.4	V
	High Level	VOH	$0.7 \cdot VDD$	-	VDD	V
Common Electrode Driving Signal	VCOM	TBD.	TBD.	TBD.	V	
Sync Frequency	FVD	TBD.	60	70	Hz	
(Panel+LSI)Power Consumption	Black Mode	-	TBD.	-	mA	

Table 4.2 LCD module electrical characteristics

**4.3 RSDS DC Electrical Characteristics**

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Output differential "high" voltage	$V_{OHDIF}$	+170	+200	+230	mV	$R_L=100\ \Omega$ $P_I=8K\ \Omega$
Output differential "low" voltage	$V_{OLDIF}$	-230	-200	-230	mV	
RSDS output common voltage	$V_{CM}$	-	1.2	-	V	

Table 4.3 RSDS DC Electrical Characteristics

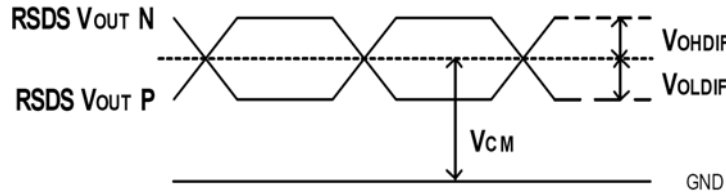


Figure 4.2 RSDS DC Timing Diagram

**4.4 Backlight Unit**

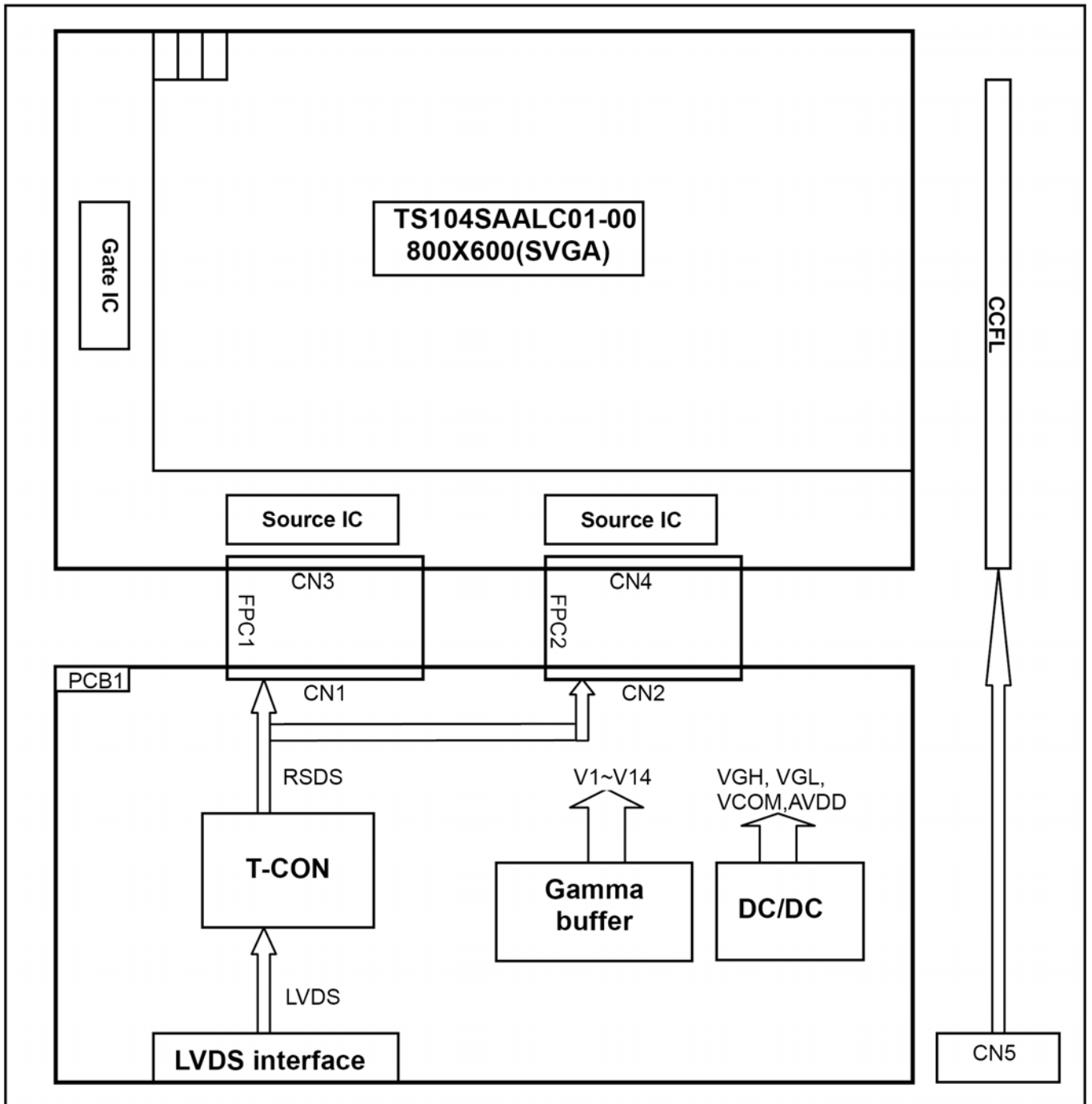
Ta=25°C

Parameter	Symbol	MIN	TYP	MAX	Unit	Remark
Lamp voltage	VL	-	520	-	Vrms	
Lamp current	IL	-	5.0	-	mA <sub>rms</sub>	
Lamp start voltage	VLS	-	-	890	Vrms	
Lamp frequency	FL	-	TBD.	-	KHz	

Table 4.4 backlight unit electrical characteristics



4. 6 BLOCK DIAGRAM



Note: FPC1 and FPC2 are physically same.

Figure 4.3 LCD module diagram



## 5 Timing chart

### 5.1 LVDS input timing:

Item	Symbol	MIN	TYP	MAX	Unit	Condition
Clock period	tLVCP	20.0	25	31.25	ns	
Clock high time	tLVCH	-	14.29	-	ns	
Clock low time	tLVCL	-	10.71	-	ns	
PLL wake-up time	tLVPLL	-	-	1	ms	
Input skew margin	tLVSKM	400	-	-	ps	f=85MHz

Table 5.1 LVDS input timing

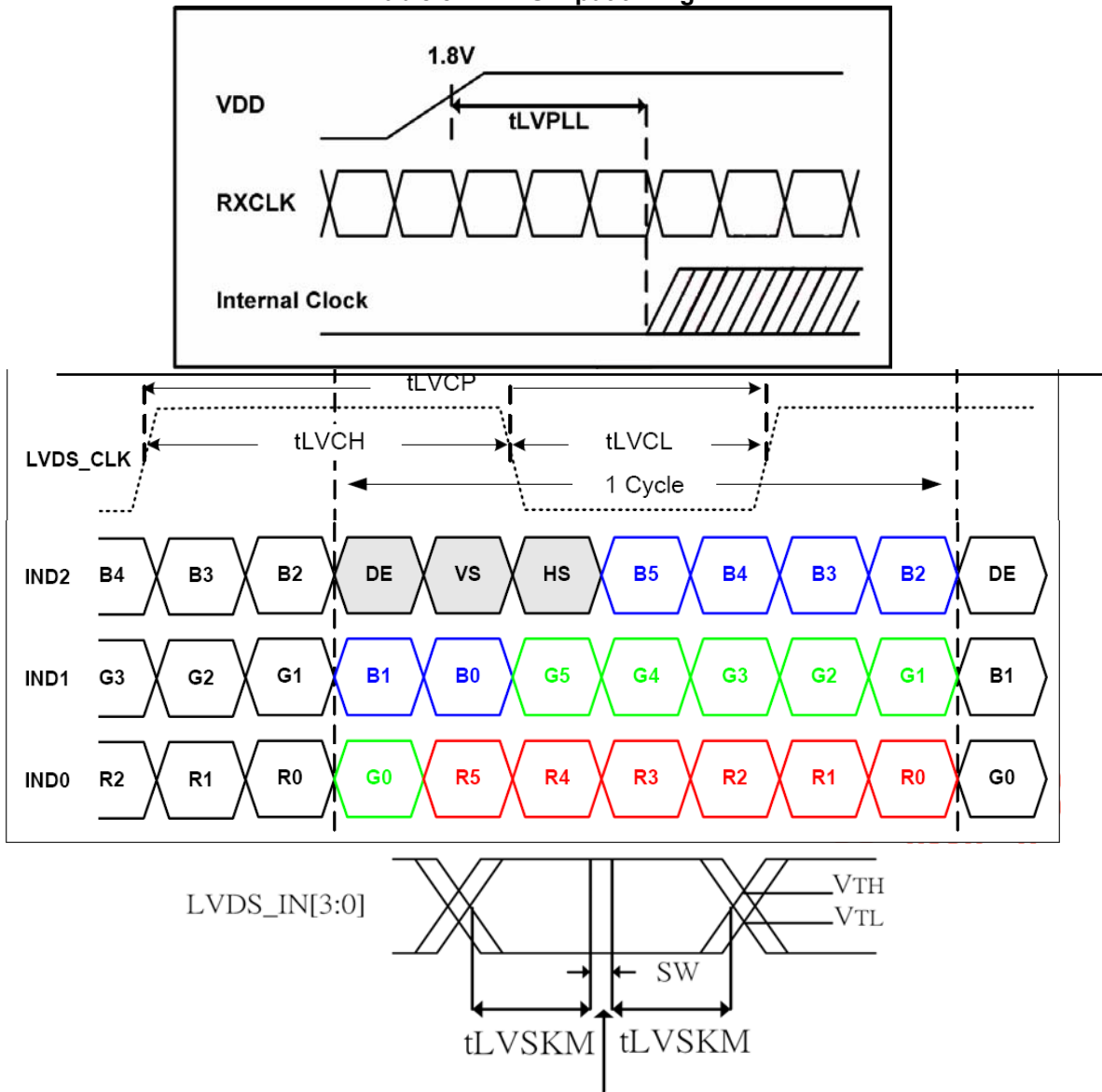


Figure 5.1 Input signal data timing

**5.2 Input Timing Control Conditions****(DE mode)**

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Frame Cycling Period	Tvp	604	628	800	Thp	
Vertical Display Period	Tw	600	600	600	Thp	
Horizontal Scanning Time	Thp	866	1056	1064	Tclk	
Horizontal Display Period	Thv	800	800	800	Tclk	
Clock Cycle	Tclk	20.0	25.0	31.25	ns	
Set-up time	Tds	0.2	-	-	Tclk	
Hold time	Tdh	0.16	-	-	Tclk	

**Table 5.2.1 Input Timing Control Conditions****(SYNC mode)**

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remarks
Hsync	Period	Thp	866	1056	1064	Tclk	
	Pulse width	Thw	12	128	128	Tclk	
	Back Porch	Thbp	12	86	94	Tclk	
	Width + BackPorch	Thw+Thbp	24	214	222	Tclk	
	Valid Data Width	Thv	800	800	800	Tclk	
	Front Porch	Thfp	42	42	42	Tclk	
Vsync	Period (Frame rate)	Tvp	70	60	50	Hz	
			604	628	800	Thp	
	Pulse Width	Tvw	2	4	27	Thp	
	Back Porch	Tvbp	0	23	172	Thp	
	Width + Back Porch	Tvw+Tvbp	2	27	199	Thp	
	Valid Data Width	Tw	600	600	600	Thp	
Front Porch	Tvfp	1	1	1	Thp		

Note: DE signal is also needed.

**Table 5.2.2 Input Timing Control Conditions**

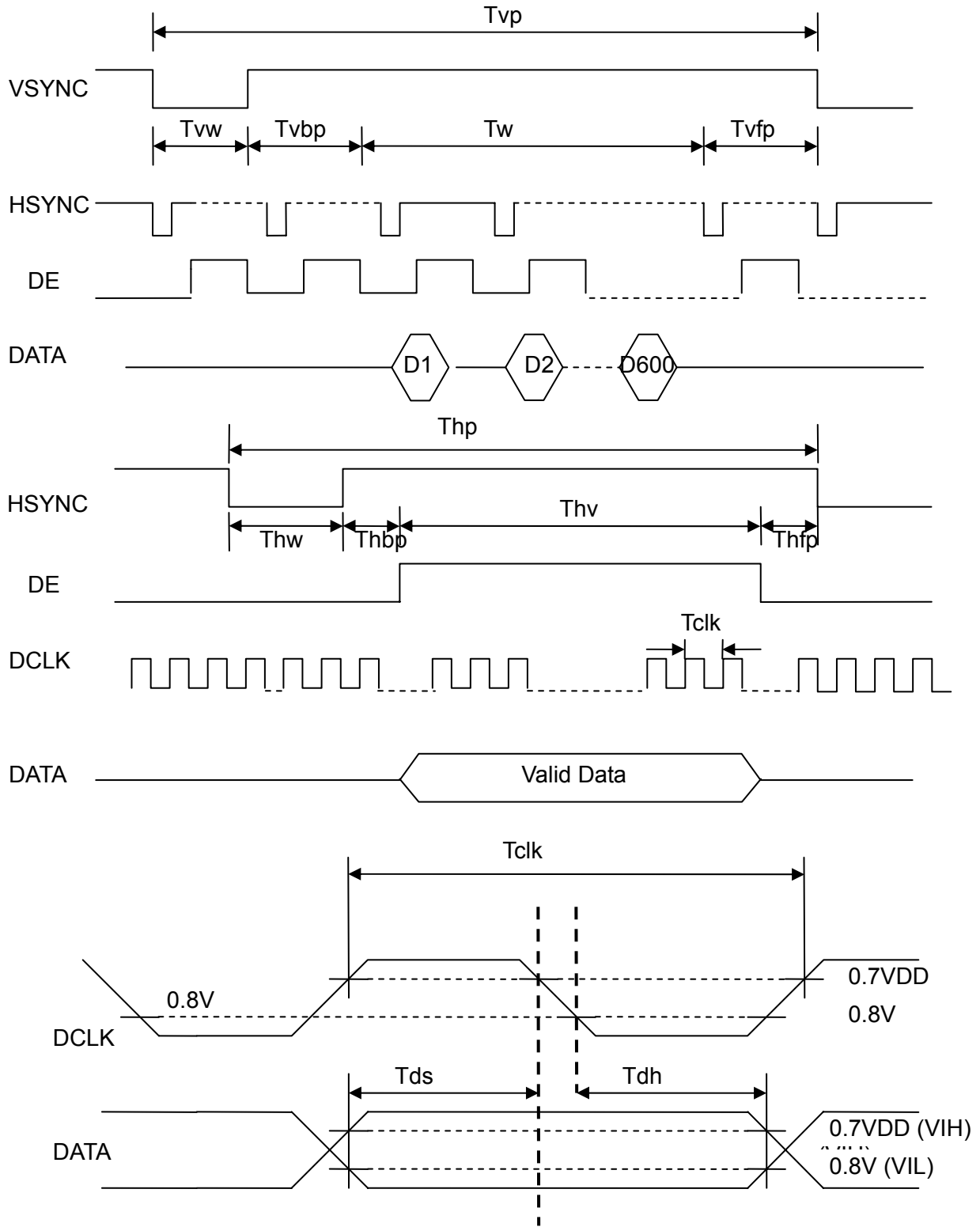
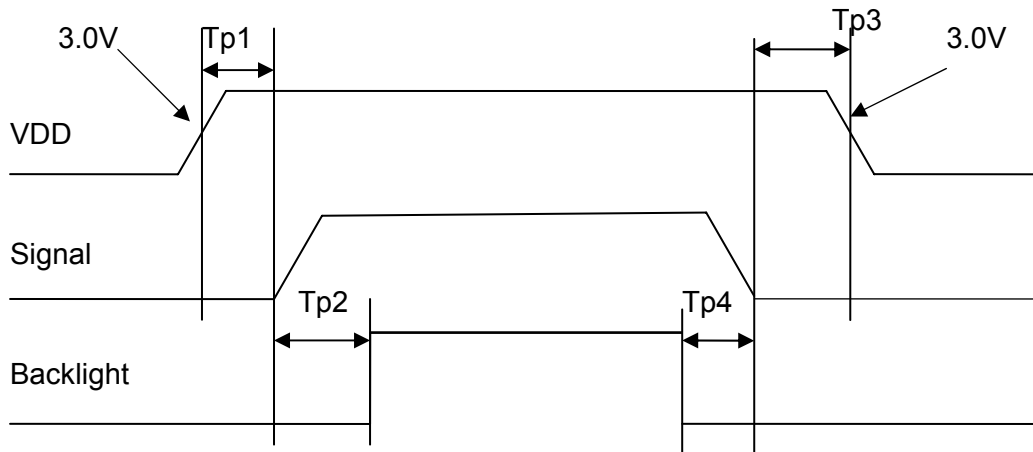


Figure 5.2 Input Timing Control Conditions

**5.3 LVDS INTERFACE POWER ON/OFF**

Item	Symbol	MIN	TYP	MAX	Unit	Remark
VDD 3.0V to signal starting	Tp1	0	TBD.	30	ms	
Signal starting to backlight on	Tp2	0	TBD	-	ms	
Signal off to VDD 3.0V	Tp3	0	TBD.	30	ms	
Backlight off to signal off	Tp4	0	TBD.	-	ms	

**Figure 5.3 interface power on/off sequence**



## 6 Optical characteristics

### 6.1 Optical Specification

Ta=25°C

Item	Symbol	Condition	Min	Typ.	Max.	Unit	Remark
View Angles	⊖ L	CR ≥ 10	55	65		Degree	Note2,3
	⊖ R		55	65			
	⊖ T		35	45			
	⊖ B		55	65			
Contrast Ratio	CR	θ = 0°		400			Note 3
Response Time	Tr	25°C		25	50	ms	Note 4
	Tf						
Chromaticity	White	Backlight on		0.310			Note 1,5
				0.330			
Uniformity	U		70	80		%	Note 6
NTSC	(x,y)			50		%	Note 5
Luminance	L		195	230		cd/m <sup>2</sup>	Note 7

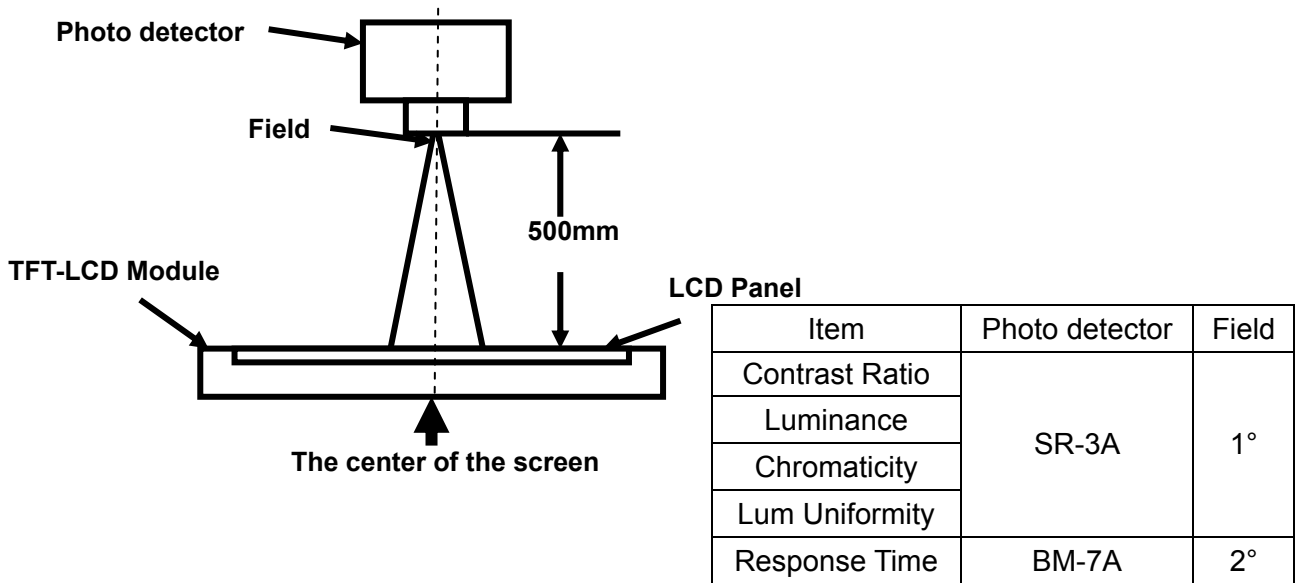
Test Conditions:

1. The ambient temperature is 25°C.
2. The test systems refer to Note 1 and Note 2.



Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80).

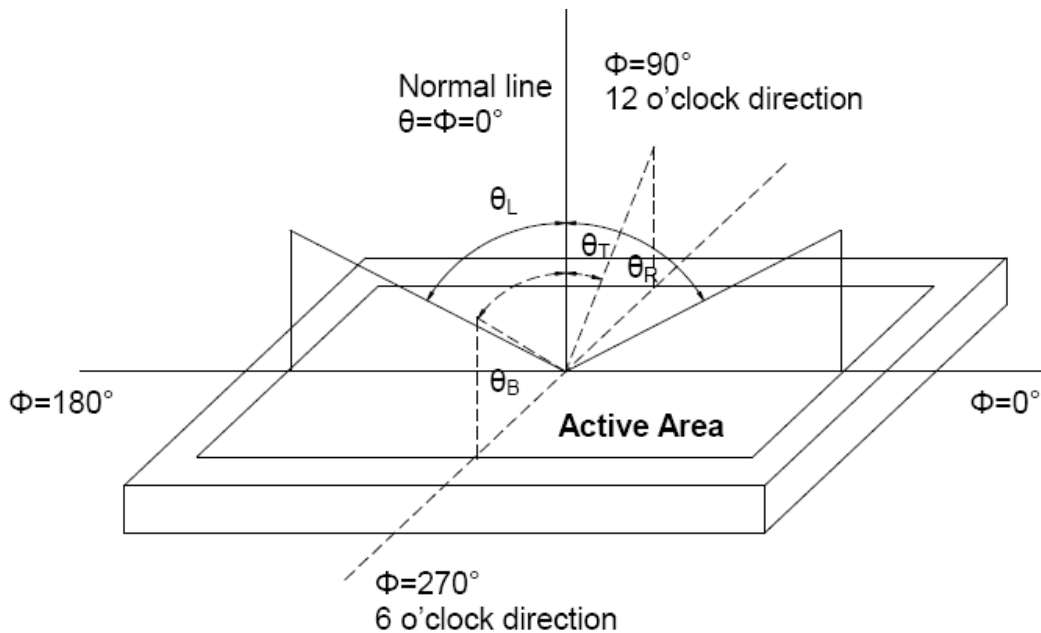


Fig. 6.1 Definition of viewing angle



Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

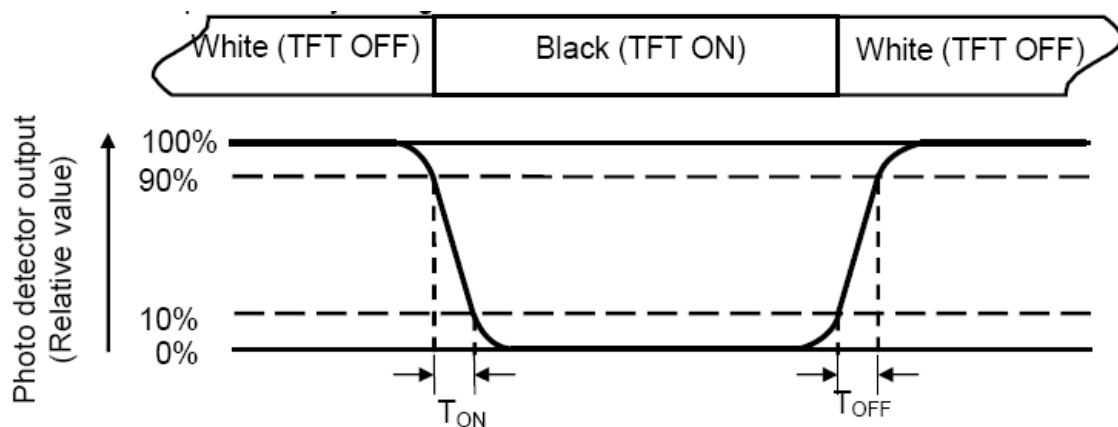
“White state “:The state is that the LCD should driven by Vwhite.

“Black state”: The state is that the LCD should driven by Vblack.

Vwhite: To be determined    Vblack: To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.



Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity}(U) = L_{\min} / L_{\max}$$

L-----Active area length W----- Active area width

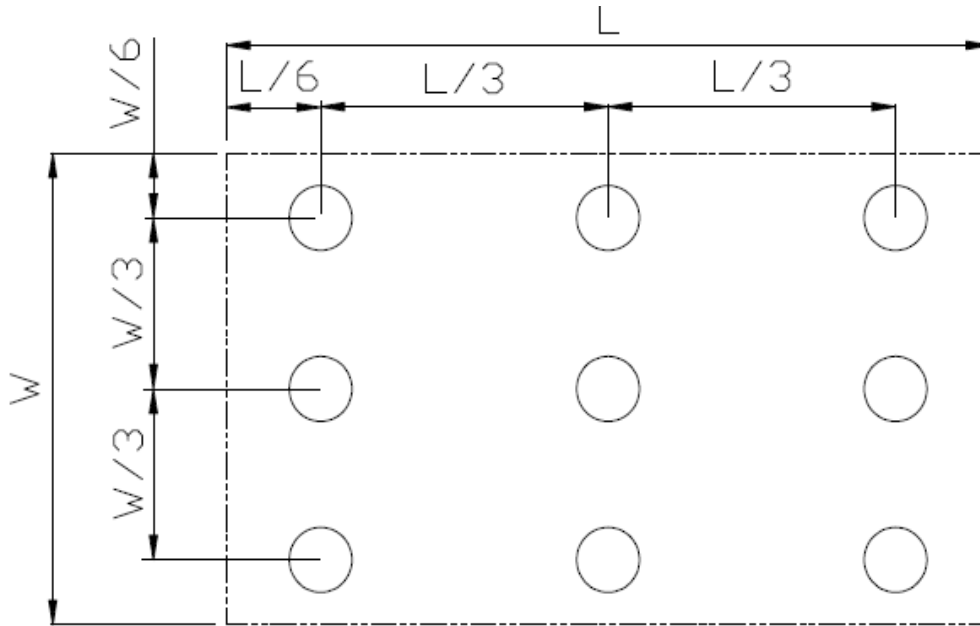


Fig. 6.2 Definition of uniformity

L<sub>max</sub>: The measured maximum luminance of all measurement position.

L<sub>min</sub>: The measured minimum luminance of all measurement position.

Note 7: Definition of Luminance :

Measure the luminance of white state at center point.

**7 Environmental / Reliability tests**

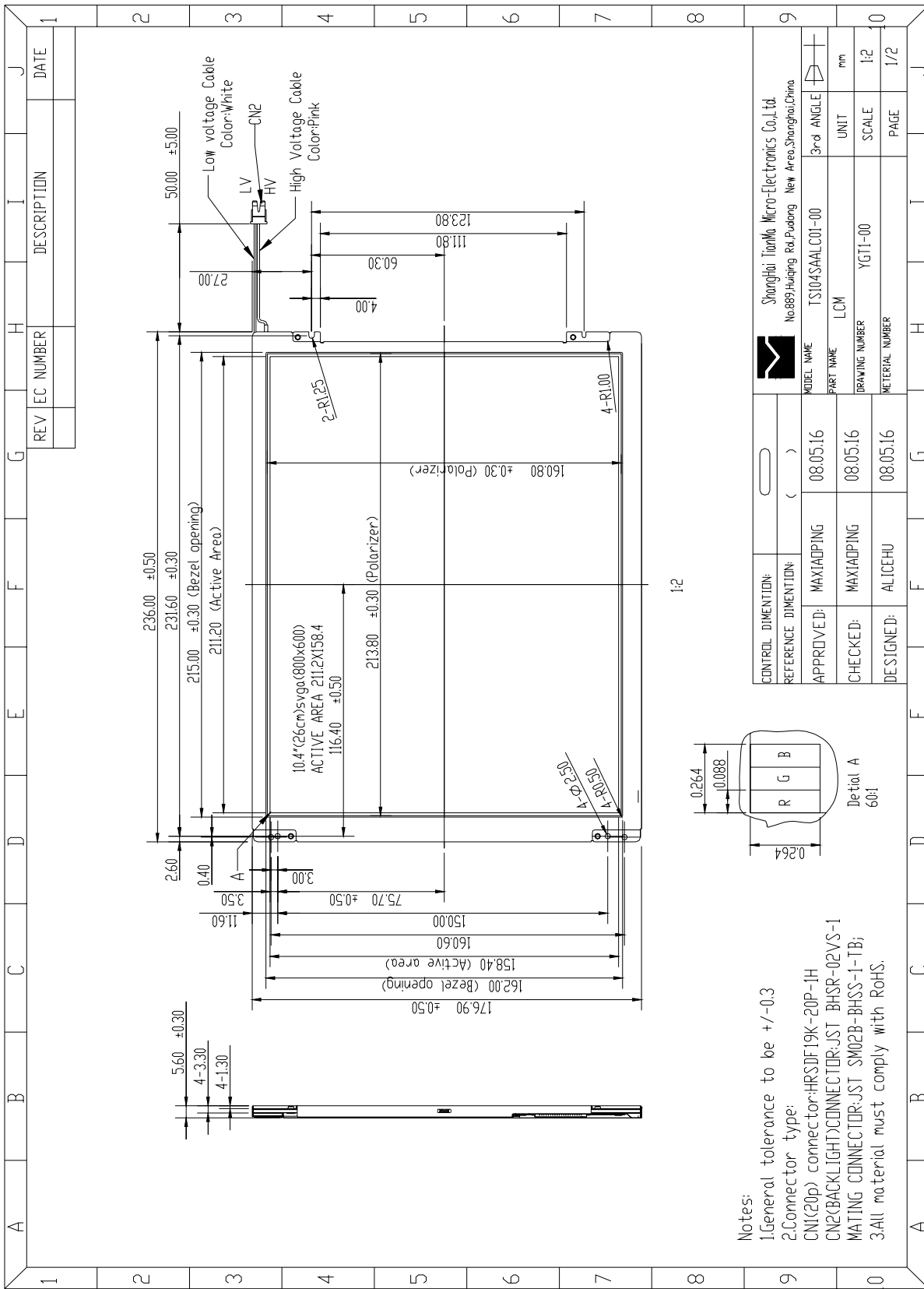
No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts=+70°C, 240hrs	Note1 IEC60068-2-2,GB2423.2—89
2	Low Temperature Operation	Ta=-20°C, 240hrs	IEC60068-2-1 GB2423.1—89
3	High Temperature Storage (non-operation)	Ta=+80°C, 240hrs	IEC60068-2-2, GB2423.2—89
4	Low Temperature Storage (non-operation)	Ta=-30°C, 240hrs	IEC60068-2-1 GB2423.1—89
5	High Temperature & High Humidity Operation	Ta = +60 °C , 90% RH max,240 hours	Note2 IEC60068-2-3, GB/T2423.3—2006
6	Thermal Shock (non-operation)	-20°C 30 min~+70°C 30 min, Change time:5min, 100 Cycle	Start with cold temperature, end with high temperature IEC60068-2-14,GB2423.22—87
7	Electro Static Discharge (operation)	C=150pF,R=330Ω, Air:±15Kv, Contact:±8Kv, 10times/terminal	IEC61000-4-2 GB/T17626.2—1998
8	Vibration (non-operation)	Frequency range:10 ~ 55Hz, Stroke:1.5mm Sweep:10Hz ~ 55Hz ~ 10Hz 2hours for each direction of X.y.z (6 hours for total)	IEC60068-2-6 GB/T2423.10—1995
9	Shock (non-operation)	80G 6ms, ±X,±Y,±Z 3times for each direction	IEC60068-2-27 GB/T2423.5—1995
10	Package Drop Test	Height:80 cm, 1 corner, 3 edges, 6 surfaces	IEC60068-2-32 GB/2423.8—1995
11	Package Vibration Test	Random Vibration: 0.015G*G/Hz for 5-200Hz, -6dB/Octave from 200-500Hz 2 hours for each direction of X,Y,Z (6 hours for total)	IEC60068-2-34

Note1: Ts is the temperature of panel's surface.

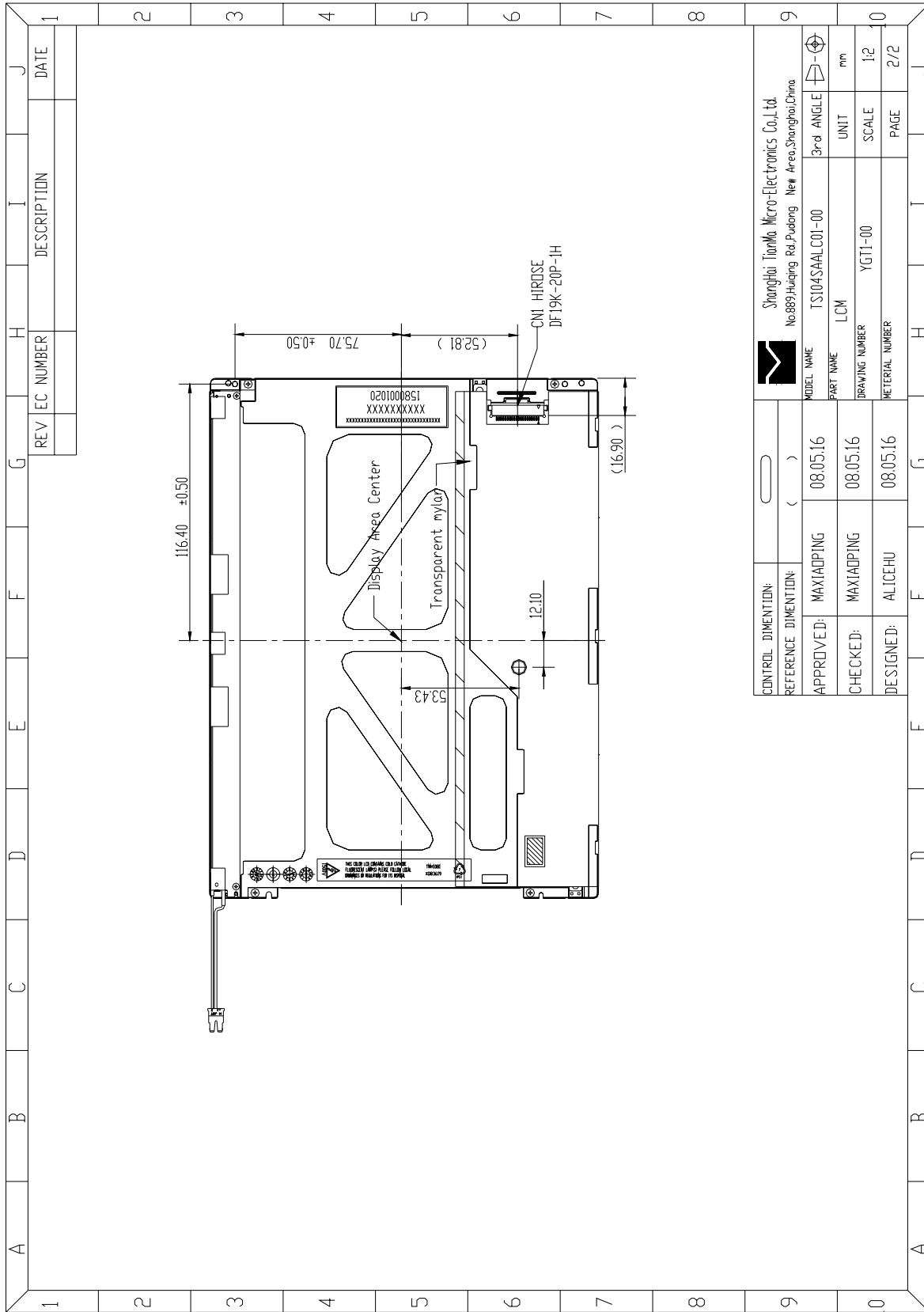
Note2: Ta is the ambient temperature of samples.



8 Mechanical drawing



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CONTROL DIMENTION:	( )	MODEL NAME	TS104SAALC01-00	3rd ANGLE	UNIT	mm	
REFERENCE DIMENTION:	( )	PART NAME	LCM	DRAWING NUMBER	YG11-00	SCALE	1:2
APPROVE D:	MAXIAOPING	08.05.16	DESIGNED:	ALICEHU	08.05.16	MATERIAL NUMBER	2/2
CHECKED:	MAXIAOPING	08.05.16					

Shanghai Tianma Micro-Electronics Co., Ltd.  
 No.889,Huajiang Rd, Pudong New Area, Shanghai, China



## 9 Packing drawing

TBD



## 10 Precautions for use of LCD modules

### 10.1 Handling Precautions

- 10.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
- 10.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.
- 10.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- 10.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.
- 10.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:
  - Isopropyl alcohol、
  - Ethyl alcohol
- 10.1.6 Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:
  - Water
  - Ketone
  - Aromatic solvents
- 10.1.7 Do not attempt to disassemble the LCD Module.
- 10.1.8 If the logic circuit power is off, do not apply the input signals.
- 10.1.9 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
- 10.2 Be sure to ground the body when handling the LCD Modules.
- 10.3 Tools required for assembly, such as soldering irons, must be properly ground.
- 10.4 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
- 10.5 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.
- 10.6 Storage precautions
  - 10.6.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.
  - 10.6.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:
- 10.7 Temperature : 0°C ~ 40°C      Relatively humidity: ≤80%
  - 10.7.1 The LCD modules should be stored in the room without acid, alkali and harmful gas.
  - 10.7.2 Transportation Precautions
- 10.8 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.